

CLAIM AMENDMENTS

1. (Currently Amended)

A control method of an MRAM (Magnetoresistive Random Access Memory) based on vertical current writing, wherein the writing operation of information in a magnetic film cell MFC of the MRAM is implemented by corporate effect of a current parallel to a surface of the MFC and vertical to an easy magnetization direction of the surface of the MFC and a part of said current being branched vertical to the surface of the MFC and passing through the MFC.

2. (Currently Amended)

An MRAM based on vertical current writing, comprising:

a) a memory control unit array composed of transistor ATR (4) units, the control unit array being integrated in a semiconductor substrate;

b) a memory cell array composed of a magnetic film cell MFC (2);

c) contact holes (3e, 3f) and a transitional metal layer, the magnetic film cell MFC (2) being connected to the transistor ATR (4) units through the transitional metal layer and the contact holes (3e, 3f); and

d) a word line WL (3d) and a bit line BL (3a), wherein

~~characterized in that~~ the bit line BL (3a) being arranged above on the magnetic film cell MFC (2), directly connected with the magnetic film cell MFC (2), and vertical to an easy magnetization direction of the magnetic film cell MFC (2) along a surface of the MFC, wherein the writing operation of the information of the magnetic film cell MFC (2) is implemented by corporate effect of a current parallel to the surface of the MFC(2) in the bit line BL (3a) and a current branched from the bit line BL (3a) vertical to the surface of the MFC and passing through the MFC.

3. (Previously Presented)

The MRAM based on vertical current writing according to claim 2, wherein one or more current-limiting mechanisms are connected to each bit line BL and are arranged in a peripheral circuit of the MRAM array.

4. (Original)

The MRAM based on vertical current writing according to claim 3, wherein the basic structure of the magnetic film cell MFC (2) is constituted by two magnetic material layers and a nonmagnetic material layer interposed between the two magnetic material layers, and stored information is

represented and stored by the magnetization state of one of the magnetic material layers.

5. (Previously Presented)

The MRAM based on vertical current writing according to claim 4, wherein the bit line BL (3a) and the word line WL (3d) are vertical to each other.

6. (Original)

The MRAM based on the vertical current writing according to claim 5, wherein the word line WL (3d) also acts as the gate of the transistor ATR (4) unit.

7. (Original)

The MRAM based on vertical current writing according to claim 6, wherein, in the process of reading information, the transistor ATR (4) is turned on and a read current is introduced from the bit line BL (3a) so as to obtain the information stored in the magnetic film cell MFC (2).

8. (Previously Presented)

The MRAM based on the vertical current writing according to claim 2, wherein there are altogether two internal metal wiring layers, i.e., a layer (5d) where the

bit line BL (3a) locates and a layer (5b) where the transitional metal layer (3b) and the ground line GND (3c) locate.

9-24 (Cancelled)

25. (Previously Presented)

The MRAM based on vertical current writing according to claim 3, wherein said current-limiting mechanism can be constituted by a diode and/or a transistor.

26. (New)

A control method of an MRAM (Magnetoresistive Random Access Memory) based on vertical current writing, wherein, during a writing operation, a part of a current on a bit line flowing parallel to a surface of a magnetic film cell MFC of the MRAM is branched to flow vertically through the MFC; and

wherein the writing operation in the MFC is implemented by a corporate effect of the current flowing parallel to the surface of the MFC and the current flowing vertically through the MFC.

27. (New)

An MRAM based on vertical current writing, comprising:

a) a memory control unit array composed of transistor ATR units, the control unit array being integrated in a semiconductor substrate;

b) a memory cell array composed of a magnetic film cell MFC;

c) contact holes and a transitional metal layer, the magnetic film cell MFC being connected to the transistor ATR units through the transitional metal layer and the contact holes; and

d) a word line WL and a bit line BL, where the bit line BL being arranged above on the magnetic film cell MFC, directly connected with the magnetic film cell MFC; and

e) a current-limiting mechanism comprising diodes and transistors on the bit line BL being arranged and integrated in a peripheral circuit of the MRAM array, where the current-limiting mechanism branches out a part of a current on the bit line BL to flow vertically through the MFC.